

LDO Voltage Regulator

Adjustable 0.45 V to 0.9 V Output, 30 mA

TSMC N3P



LDO Voltage Regulator, 30 mA, Adjustable 0.45 V to 0.9 V Output

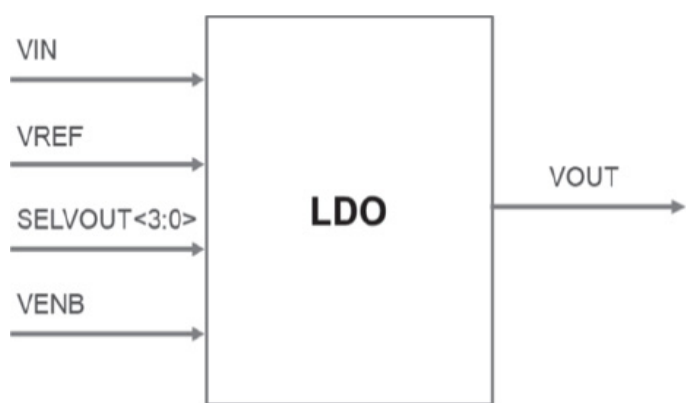
The LDO IP is a 1.2V low-quiescent-current adjustable output voltage Low-Drop-Out (LDO) Linear Regulator implemented in the TSMC 3nm N3P CMOS process technology. Its low sleep current, 30 mA maximum current, output voltage adjustability and precision make it especially suitable for use as an integrated voltage regulation source for subsystems implemented in analog, digital, mixed-signal and RF ASICs and SoCs.

Features

- TSMC 3nm FinFET process
- Input voltage: 1.2 V
- Output voltage range: 0.45 V to 0.9 V
- Vout adjustable in 50 mV increments
- Load current: 30 mA (max)
- PSRR:
 - > 40 dB @ 1 KHz
 - > 29 dB @ 10 MHz
- < 18 mV undershoot/overshoot for load transients 1 A/ ns
- Compact area – 3400 sq um
- Capless stable operation
- Functional from -40°C to 125°C
- Speed / Static Power tradeoff option

Deliverables

- SPICE netlist
- GDSII
- Behavioral Model
- IP Datasheet
- User's Guide



Specifications

Silvaco LDO	Values			
	Minimum	Typical	Maximum	Units
Core Supply Voltage	1.08	1.2	1.32	V
Output Current Capability			30	mA
PSRR (1 KHz)	40	49	60	dB
PSRR (10 MHz)	29	38	45	dB
Silicon Area		3400		um ²